[Time: Three Hours]   **[Marks:80]**

Please check whether you have got the right question paper.

1. **Question No. 1 is compulsory.**
2. **Out of remaining questions, attempt any three questions.**
3. **Assume suitable additional data if required.**
4. **Figures in brackets on the right hand side indicate full marks.**

1. (A) Compare Combinational circuits with Sequential circuits.   (05)
   (B) Compare TTL with CMOS logic families.   (05)
   (C) Compare Synchronous counter with Asynchronous counter.   (05)
   (D) Compare Moore machine with Mealy machine.   (05)

2. (A) Implement the following Boolean equation using single 4:1 MUX and few   (10)
        logic gates:
        $F(P,Q,R,S) = \Pi M(0, 2, 5, 6, 7, 9, 12, 15)$
   (B) Convert T type flip flop into D type flip flop.   (05)
   (C) Implement $Y = (\overline{A} + B)(\overline{A} + \overline{C})$ using only NAND gates.   (05)

3. (A) Write the VHDL code for counter with negative edge triggered clock and   (10)
        active low Preset and Clear terminals to count a sequence:
        $1 \rightarrow 3 \rightarrow 5 \rightarrow 7 \rightarrow 1$
   (B) State and prove the De Morgan's theorem.   (05)
   (C) Draw the internal logic diagram of Programmable Logic Array (PLA).   (05)

4. (A) Design synchronous counter using T type flip flops for getting the following   (10)
        sequence: 1   3   5 → 7 → 1 →   →
        Take care of lockout condition.
   (B) Compare SRAM with DRAM.   (05)
   (C) Write $(FF)_{16}$ into its Binary code, BCD code, and Octal code.   (05)

5. (A) Draw a neat circuit of BCD adder using IC 7483 and explain.   (10)
   (B) Using Quine McClusky method, minimize the following: (10)
        $F(X,Y,Z) = \sum m(0, 2, 4, 6) + d(1, 3, 5, 7)$.

6. (A) What is shift register? Explain any one type of shift register. Give its   (10)
        application.
   (B) Design a Mealy type sequence detector circuit to detect a sequence 1101   (10)
        using T type flip flops.

****